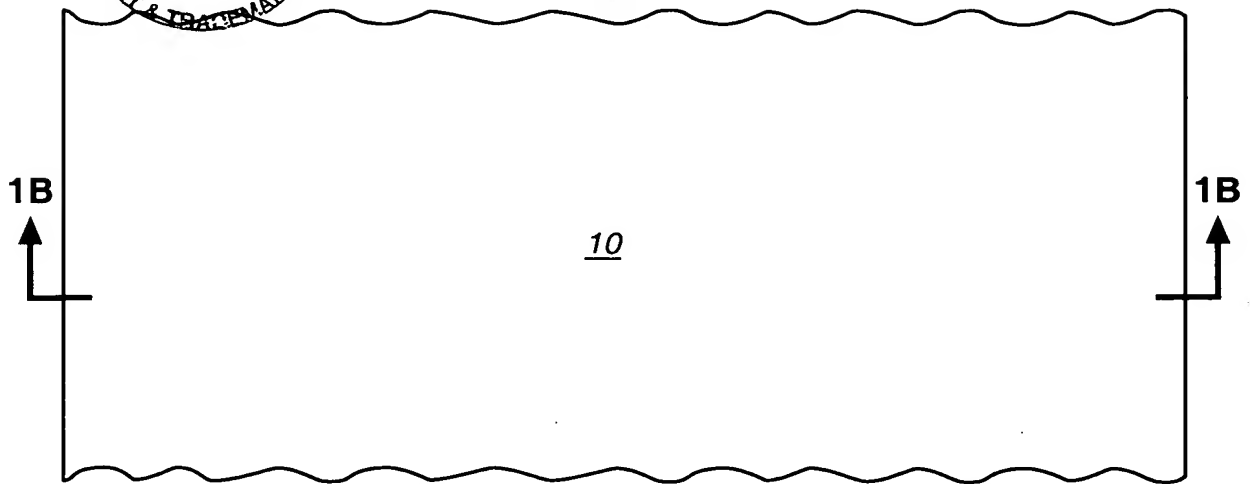


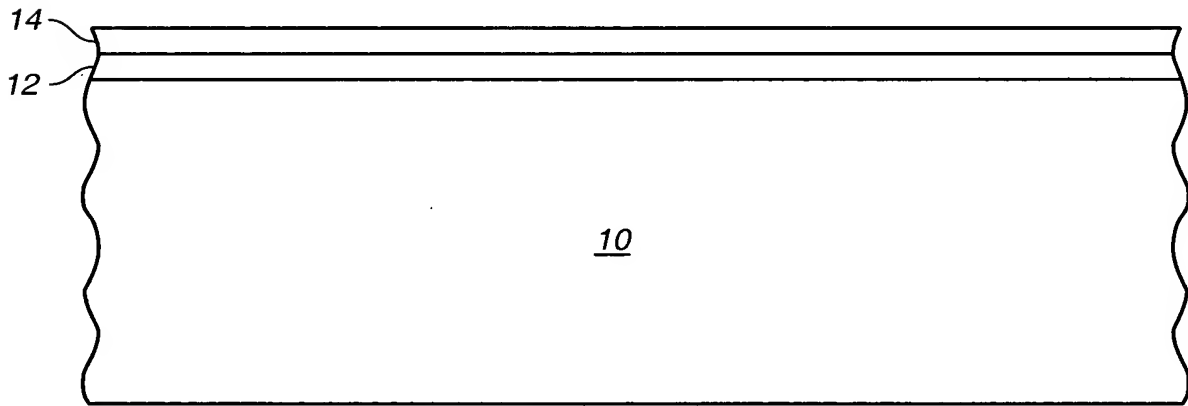


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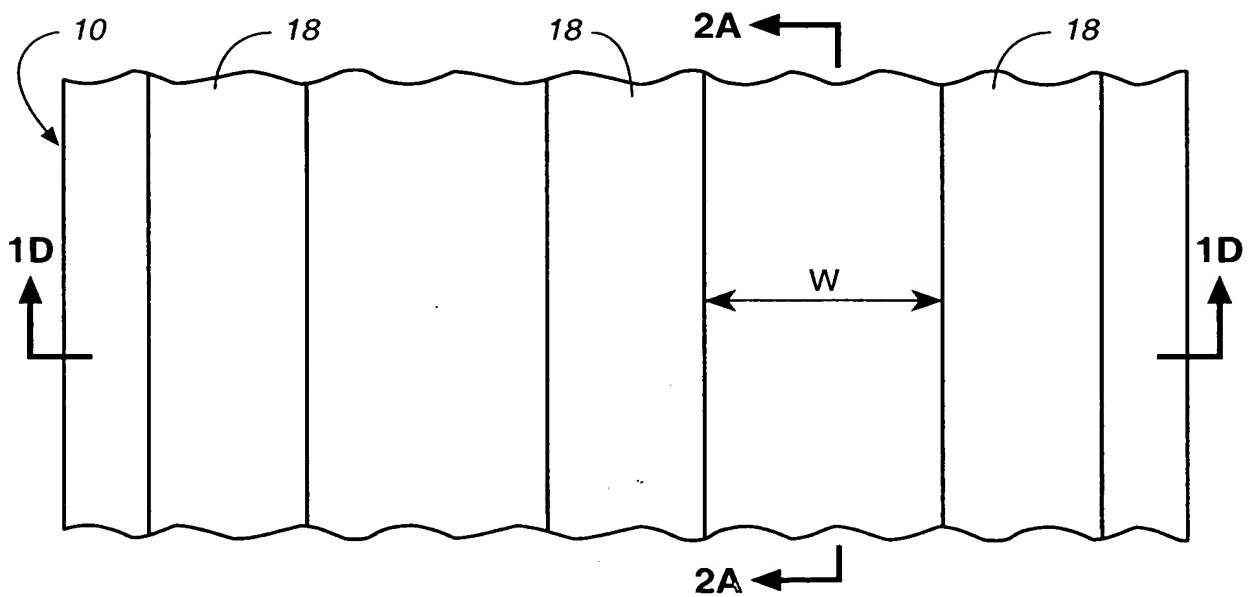
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**FIG.\_1A**

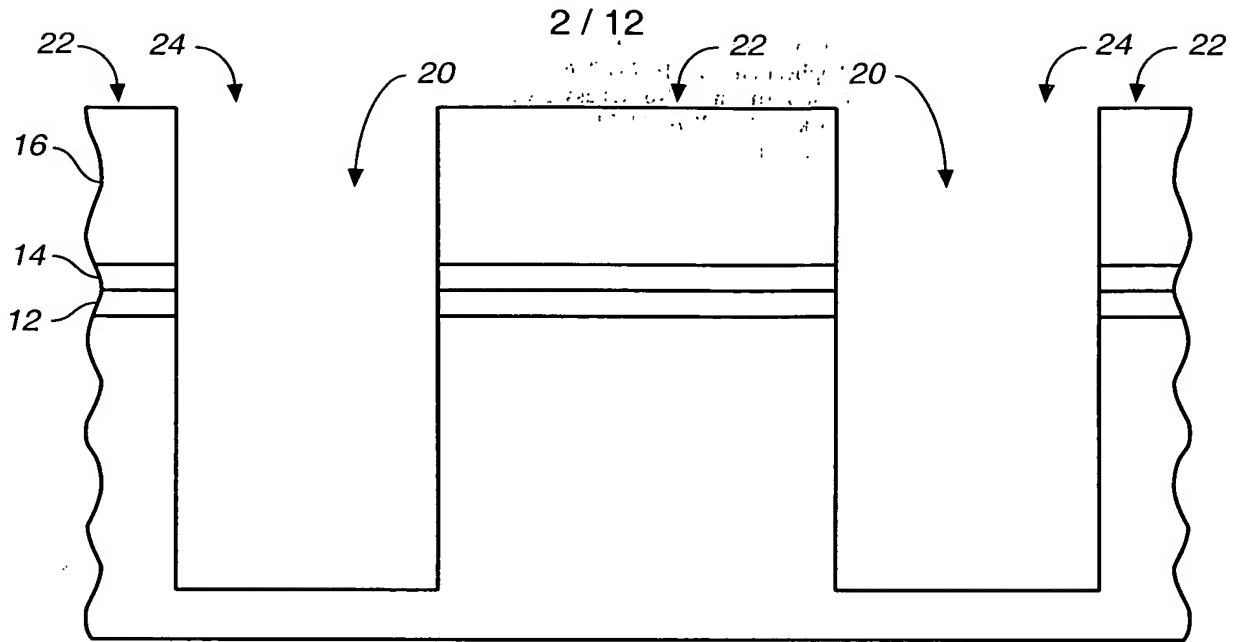


**FIG.\_1B**

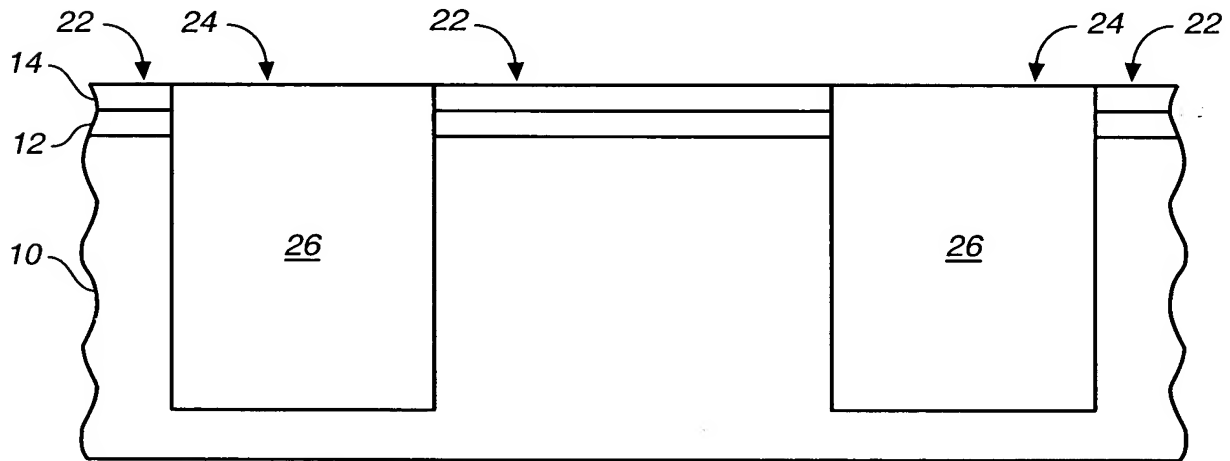


**FIG.\_1C**

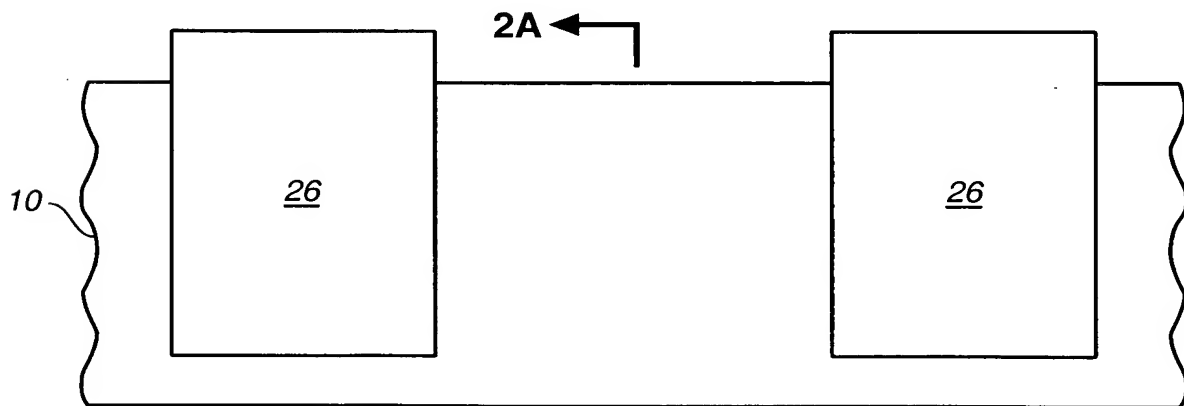
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**FIG.\_1D**



**FIG.\_1E**

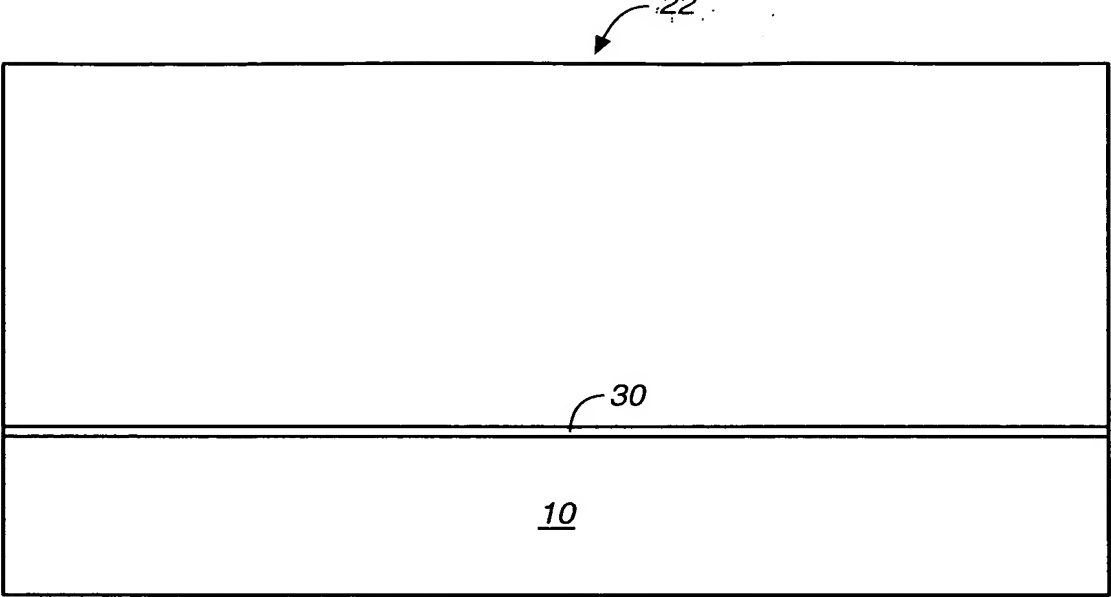


**FIG.\_1F**

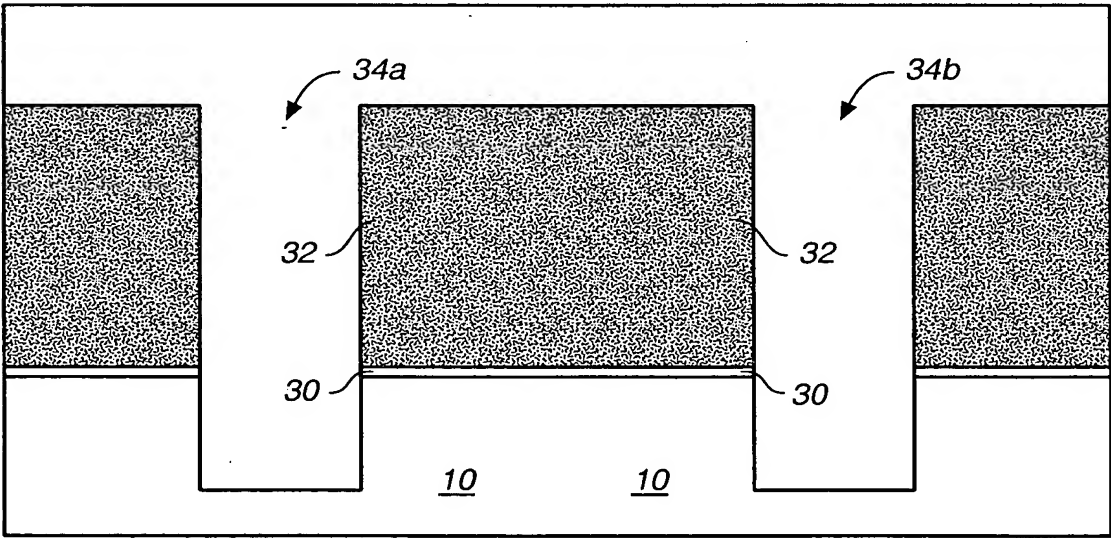


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FIG. 2A is a schematic diagram of a device 10 in a first state. The device 10 includes a substrate 10 and a layer 30 disposed on the substrate 10. The layer 30 includes a portion 22.

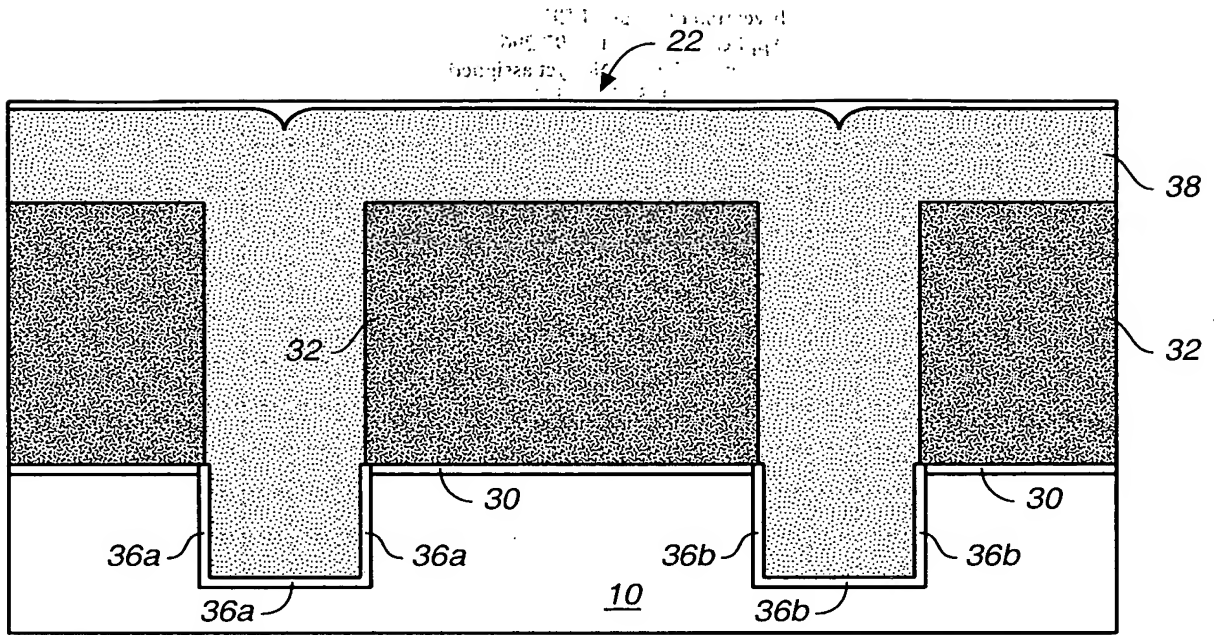


**FIG. 2A**

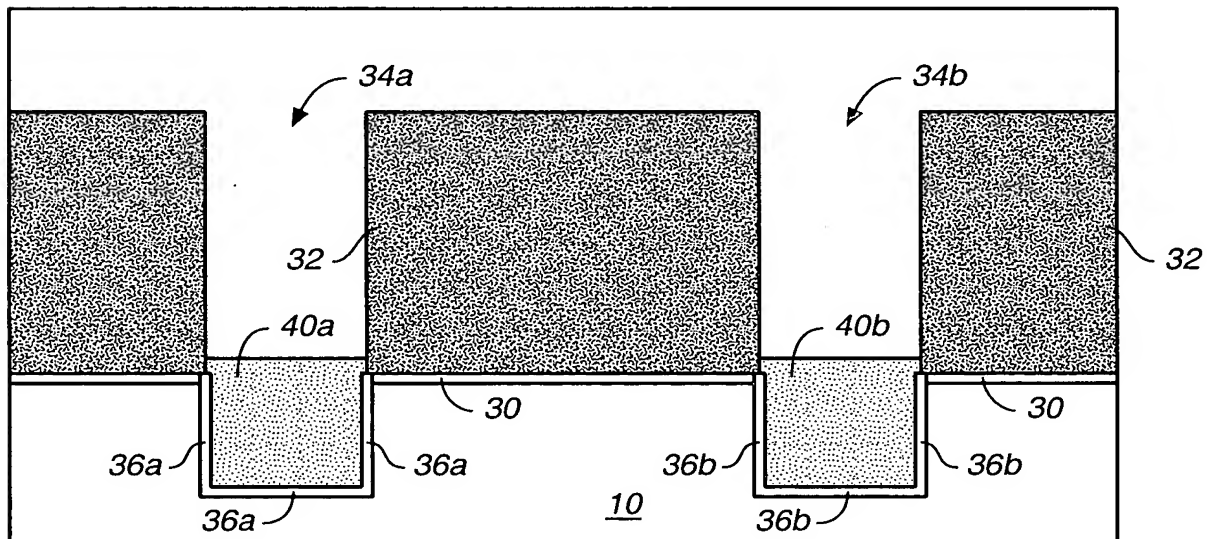


**FIG. 2B**

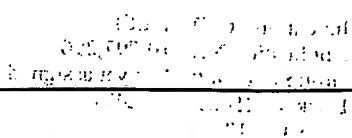




**FIG. 2C**



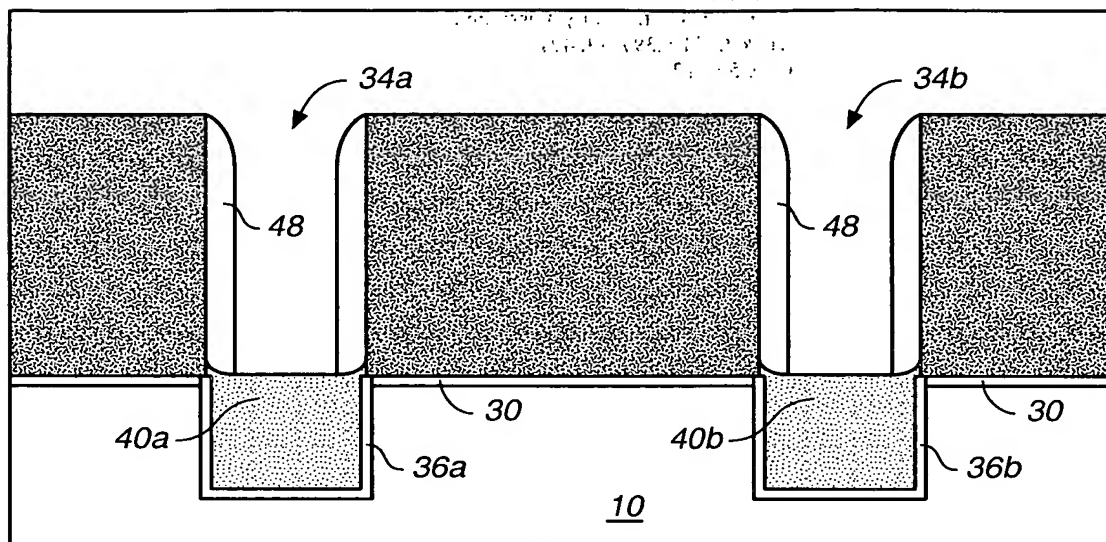
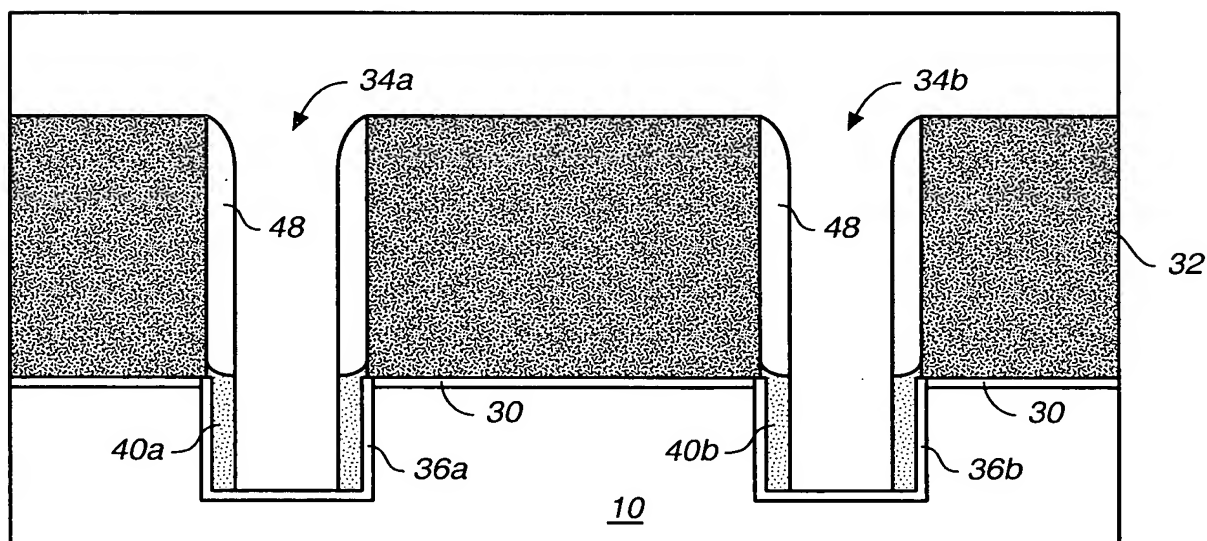
**FIG. 2D**

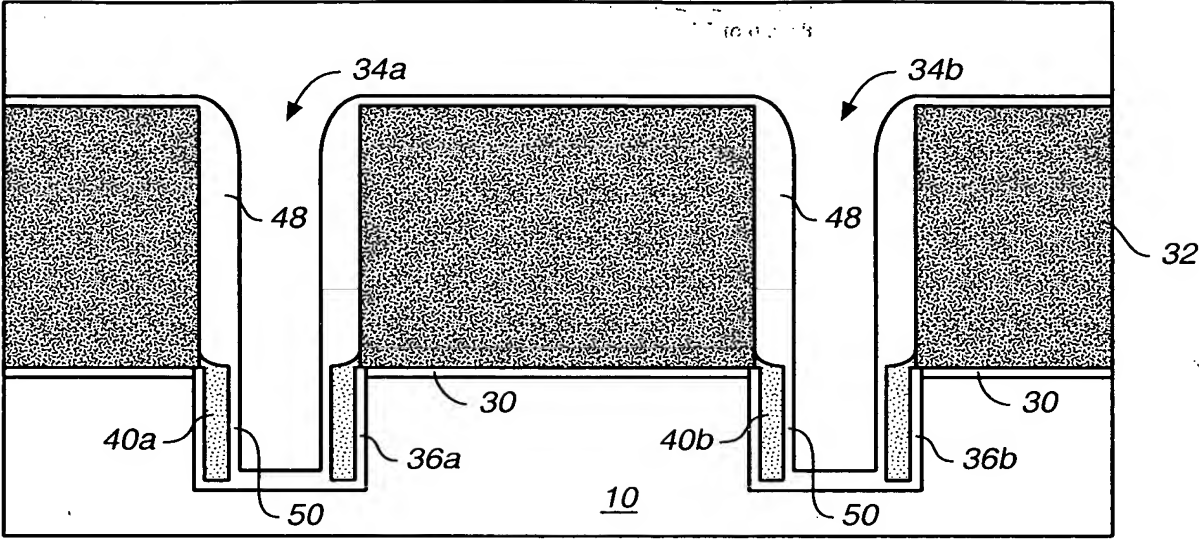


3

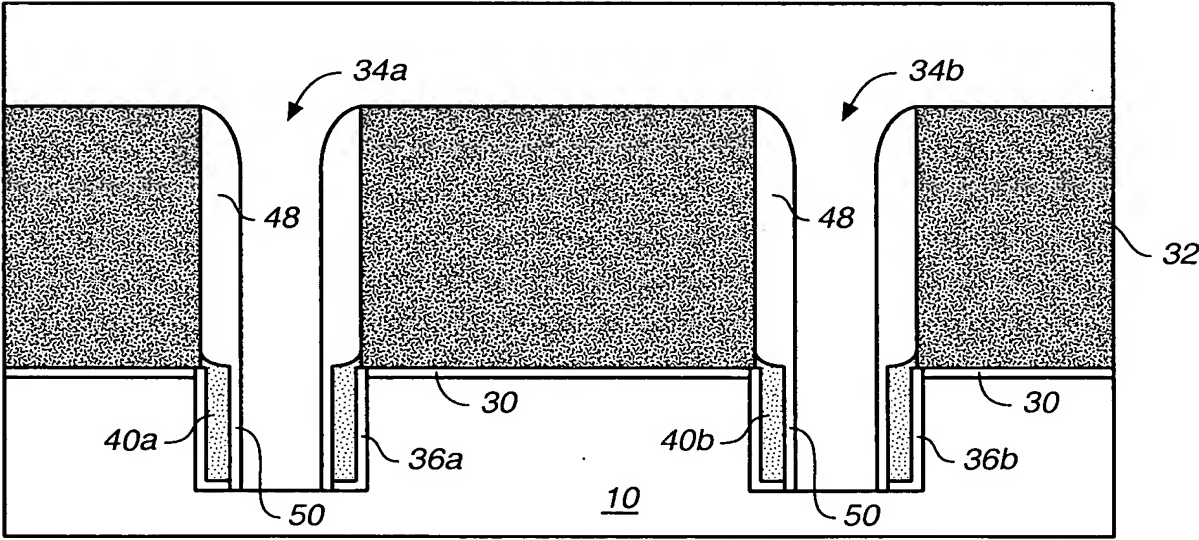


+

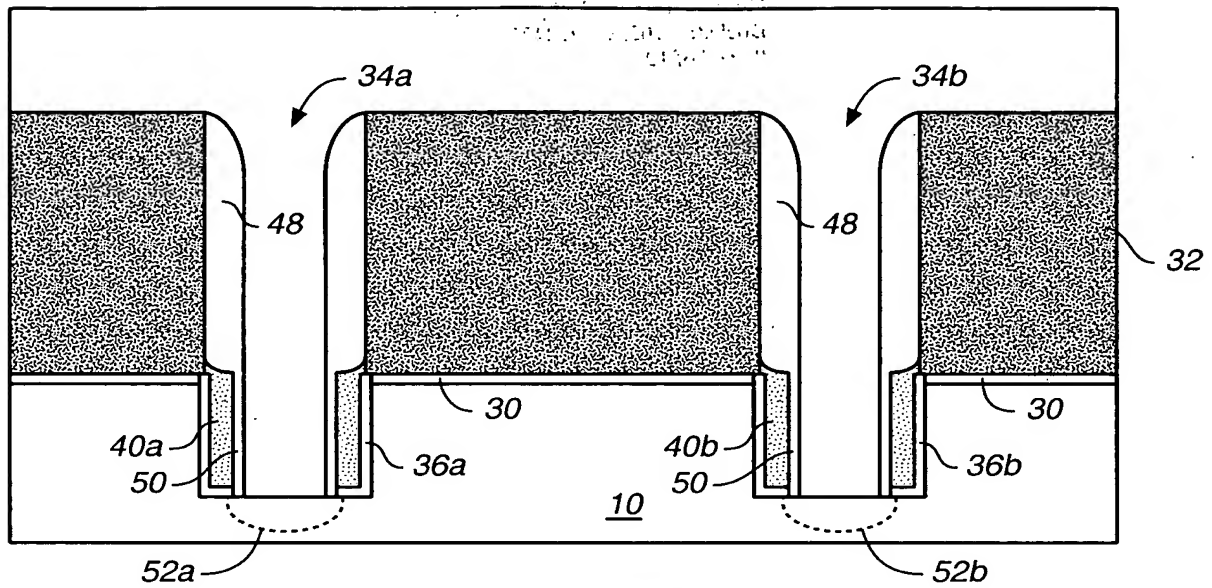
**FIG. 2G****FIG. 2H**



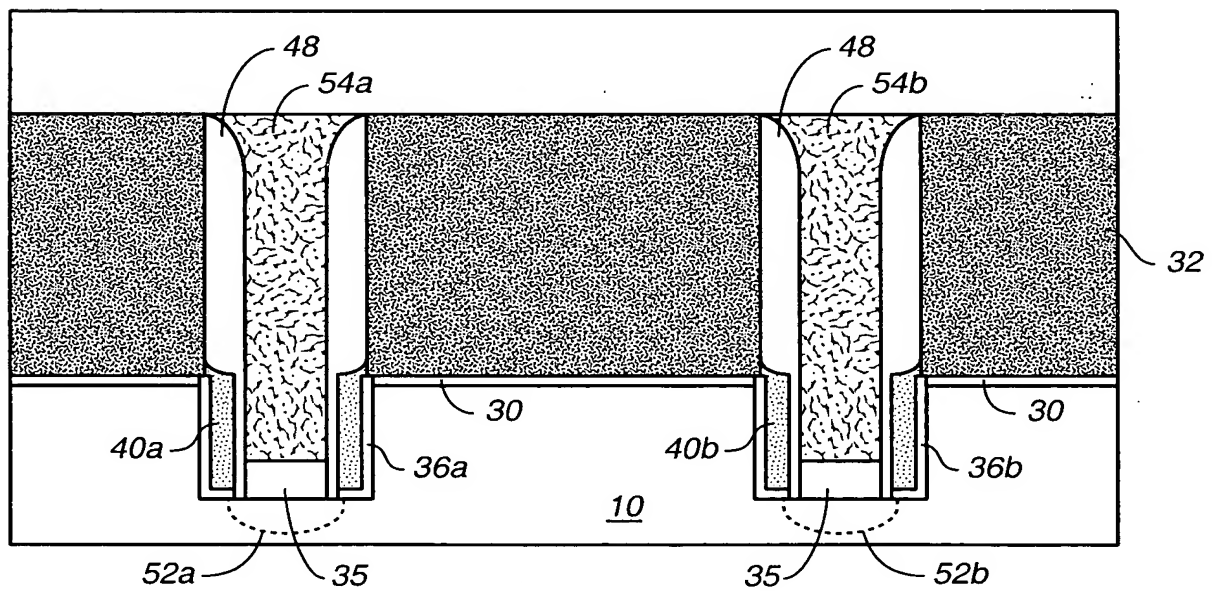
**FIG. 2I**



**FIG. 2J**

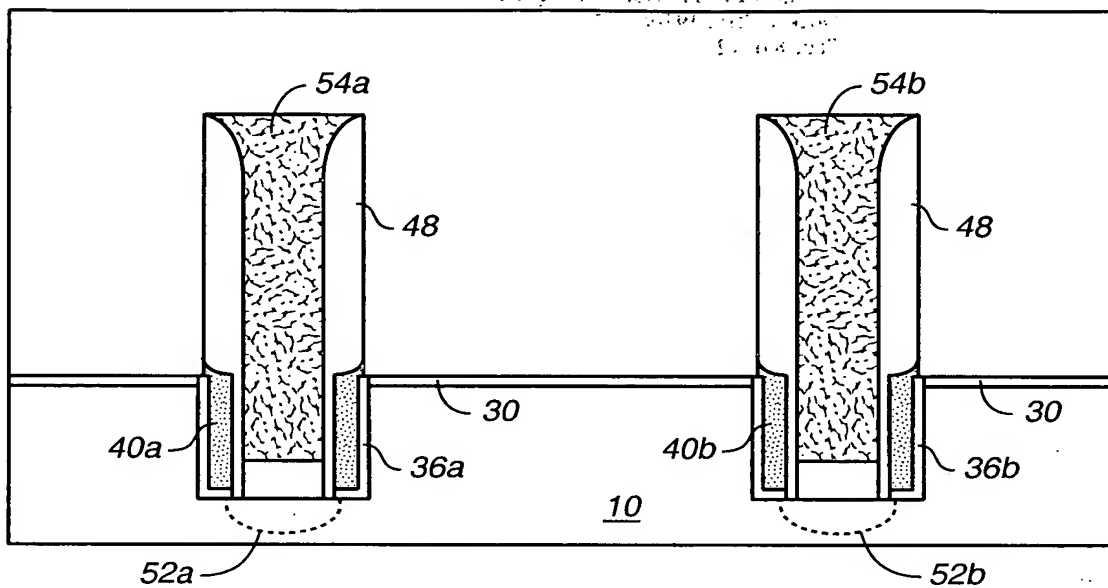
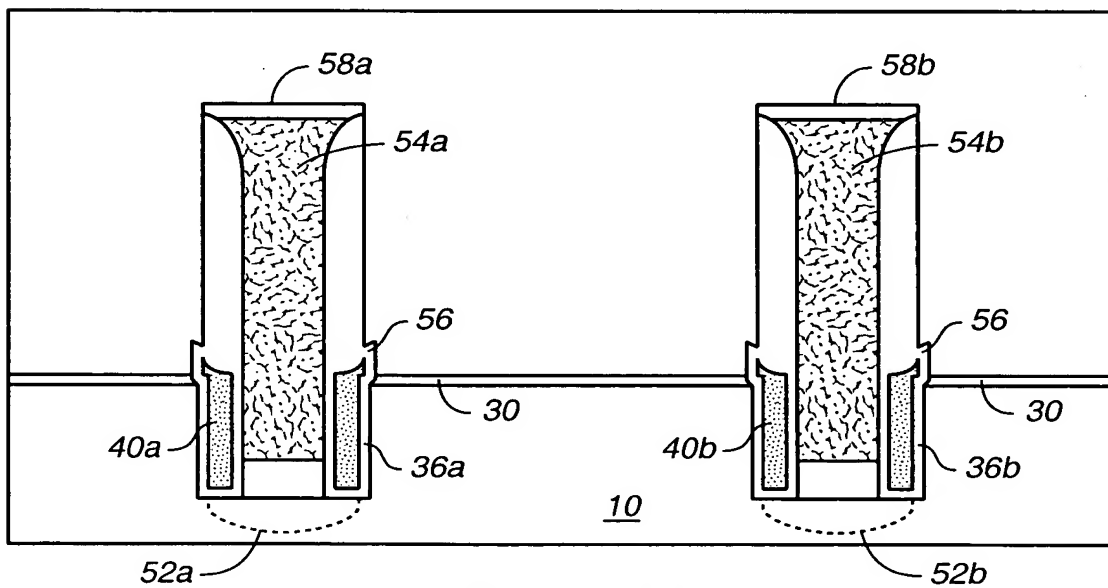


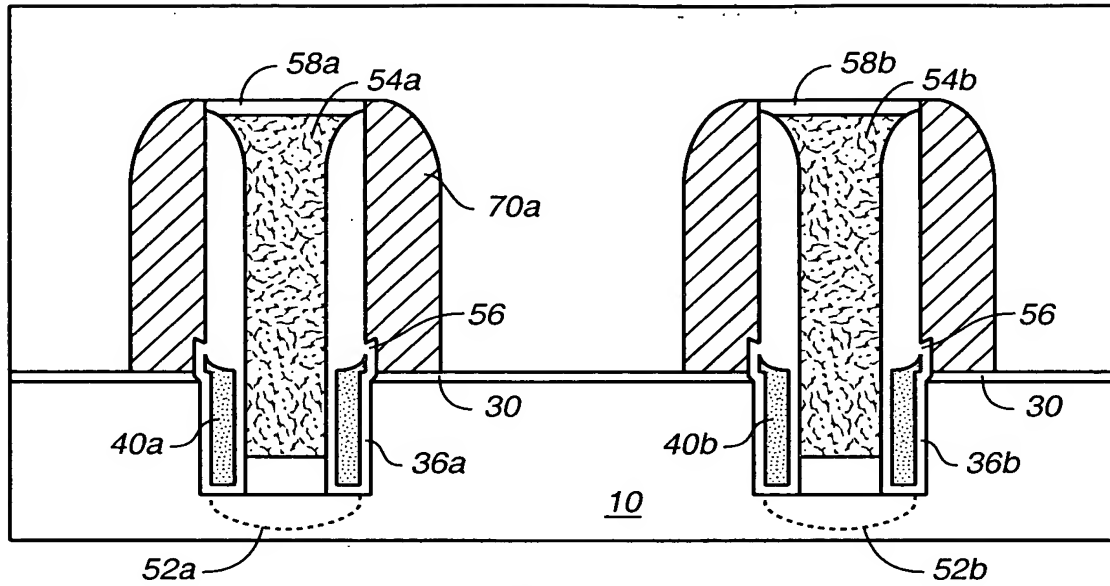
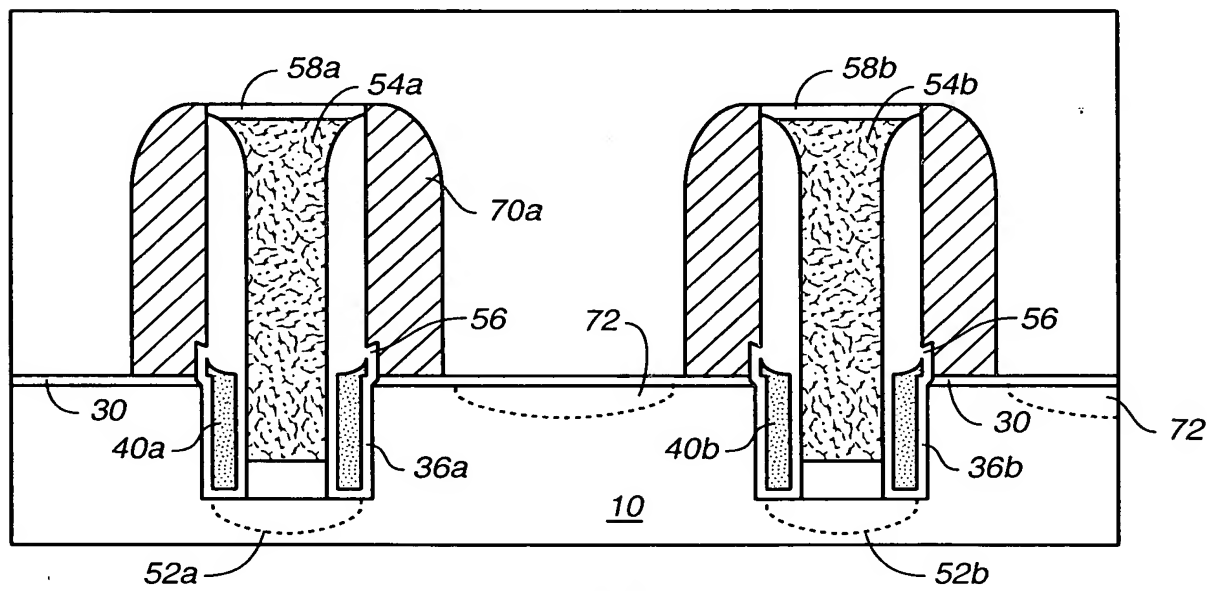
**FIG.\_2K**



**FIG. 2L**



**FIG.\_2M****FIG.\_2N**

**FIG. 20****FIG. 2P**

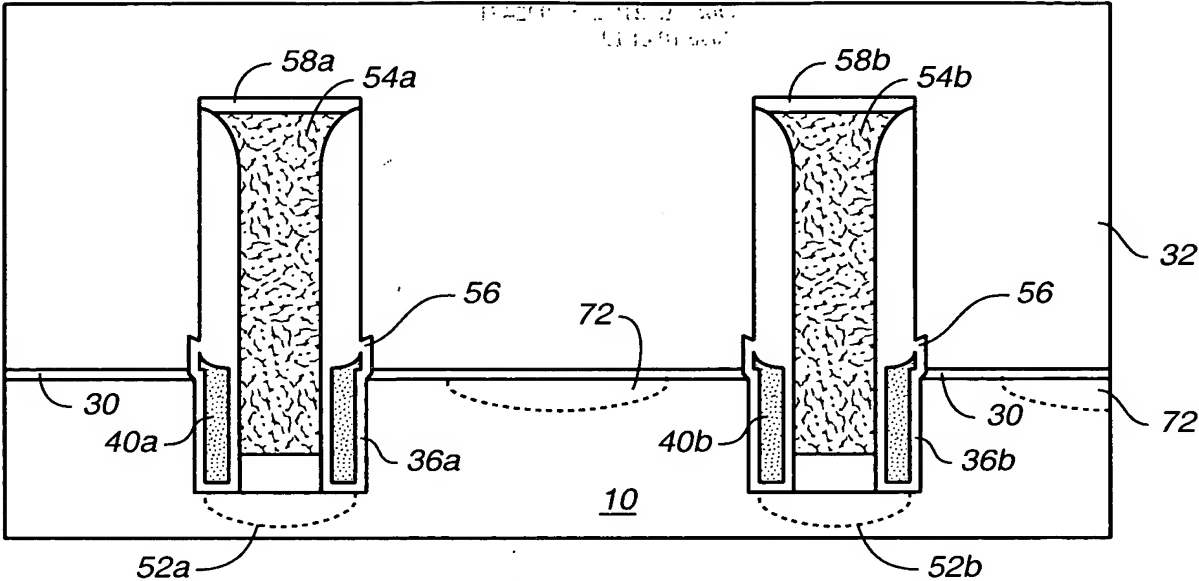


FIG.\_2Q

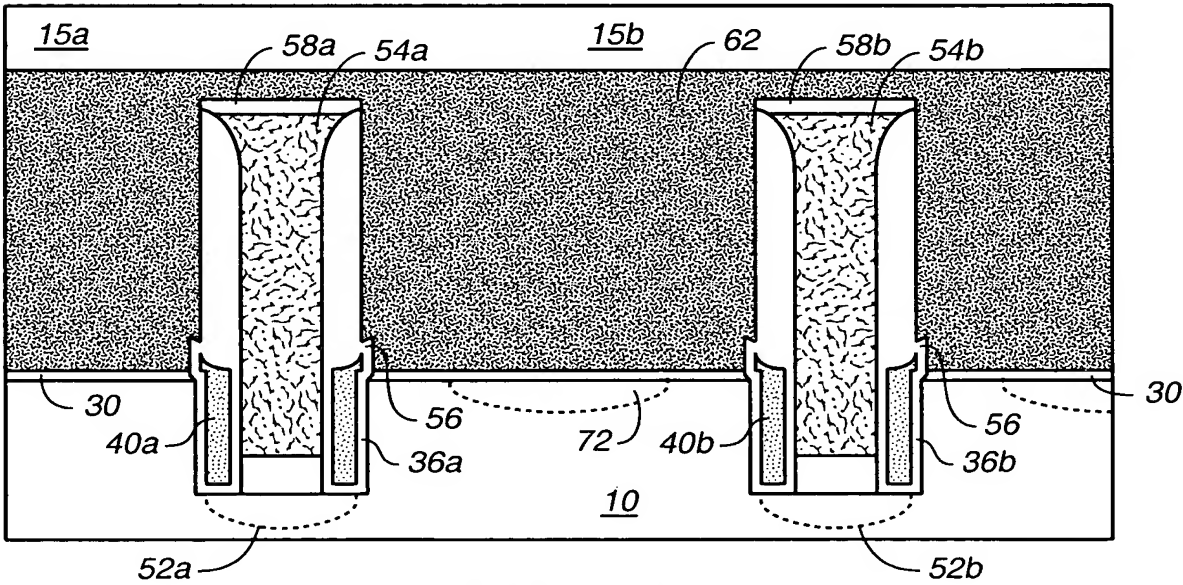
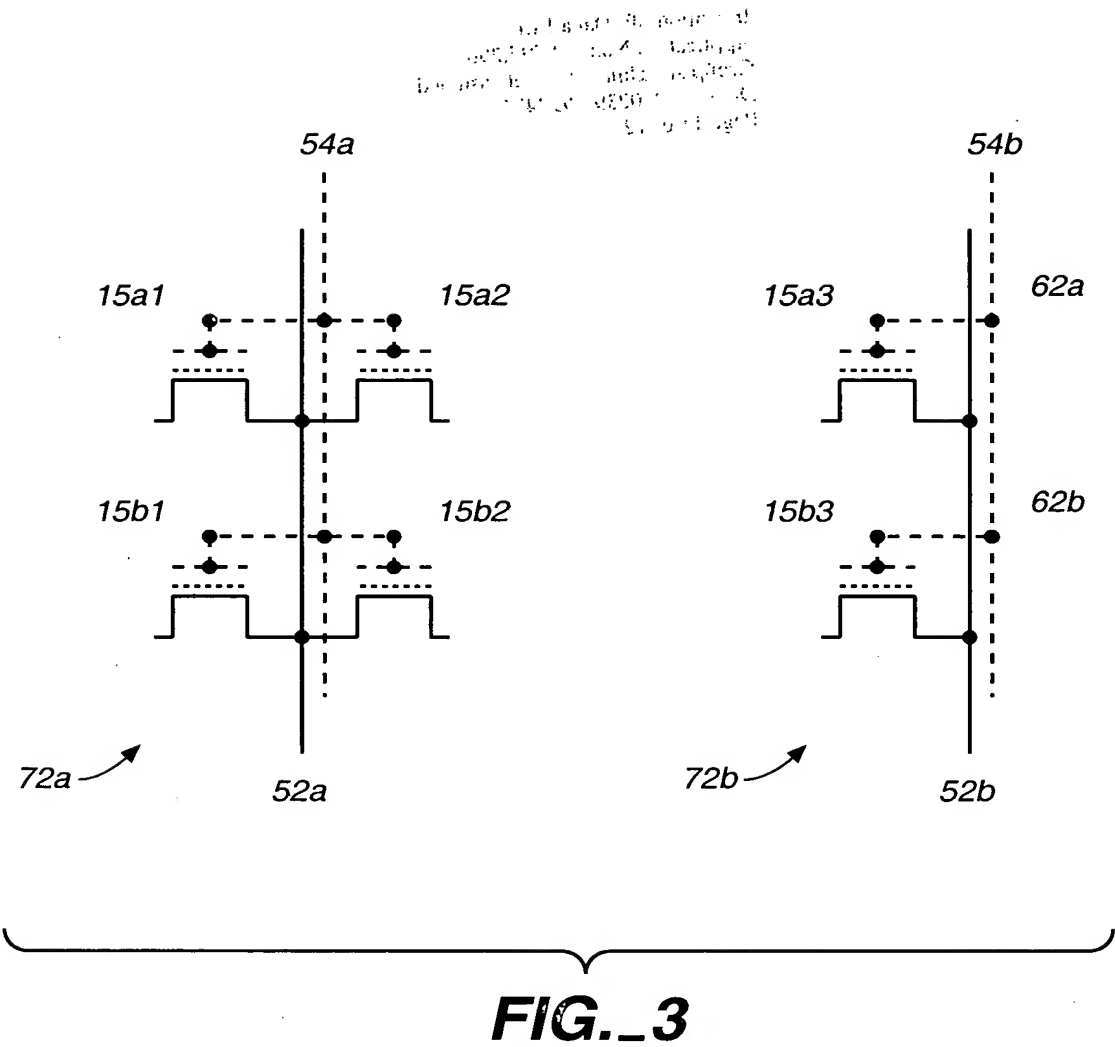


FIG.\_2R



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